K 202 HANDBOOK

1. INTRODUCTION

K 202 is a fourth generation computing system based on a fast, asynchronous processor having a sixteen bit word length and a dual bus which provides for very comprehensive bulk storage and input/output facilities.

Hardware and software are completely modular, and can be assembled into any configuration from a mini-computer with 4K store and one input/output device, to a large multi-processor system having hardware floating point units, up to four million words of directly addressable core store, and an almost unlimited number of peripheral devices. Bulk storage peripherals all have autonomous data transfer facilities, and all input/output devices work on a time-sharing basis. All peripherals have individual interrupts, with hardware pointers to their interrupt routines.

Thirty two levels of interrupt in the basic machine provide very powerful facilities: multi-programming is a feature of all systems having more than one block of core store; multi-access is inherent in any system having more than one input/output peripheral.

The processor provides seven universal registers which serve as accumulators, indexes, pointers etc. A unique and sophisticated control logic combines fail-safe and auto-diagnostic properties with an economy of components which keeps the cost below that of machines offering less facilities.

A comprehensive range of software includes an Operating System, which combines an Executive program with Maths, Peripheral and Error routines; the ASSK Assembler; and compilers for BASIC, FORTRAN IV, ALGOL 60, and C.S.L. high level languages. A wide range of applications programs is available to all users.

2. THE OVERALL SYSTEM

This section describes how the K-202 system is completely modular and can be built up from a minimum to a maximum system by simply plugging in the extra modules. It also describes the multi-programming and multi-access facilities which are inherent in the system, and explains the advantages of operating two or more processors on a common data highway.

2.1 MODULAR STRUCTURE

The K-202 system is completely modular, and may be built up from a minimum to a maximum system by simply plugging in extra modules. Systems software is also modular, and with each additional item of hardware is supplied the necessary software routines to update the operating system programs to cater for the new devices.

It is not necessary to switch off an installation ~~for a short time~~ whilst connecting new modules, and once connected it is usual to run systems tests before bringing the equipment back into service. However, the total time consumed in this procedure tends to be less than ~~an~~ a quarter of an hour. It is never necessary to return equipment to the factory in order to add new modules.

The minimum system consists of the processor with operators control panel and power supplies, coupled to 4096 words of read/write core store, and one input/output device such as a teleprinter. Apart from the teleprinter, this whole system is built into a single case size (19"x8½"x22") or may be mounted in a standard 19" rack. Also included in the basic unit are the controller and connectors for three further input/output devices, room to expand the internal store to 16K words, and space for a fast F.P arithmetic unit and bus connections to facilitate expansion up to the maximum system.

2.3 MAXIMUM SYSTEM

The maximum system includes the whole of the minimum system, plus a fast FP arithmetic unit; sixty-~~four~~ three CORE STORE MODULES AND 64 BULK storage AND PERIPHERALS process control modules connected to the store bus, and sixty-~~four~~ three input/output modules connected to the input/output bus.

Modules which may be connected in any combination to the store bus include:-

1. Additional core stores, each having 16K to 64K words of 16 bits, and read/write cycle time of 0.7 uS or 1.2 uS.
2. Bulk storage such as magnetic disc, drum or tape units as listed in section 3.6.1. For every group of eight such units, a store controller is required.
3. Multiplexors, each providing up to 32K inputs and/or outputs of 16 bits for process control.

Modules which may be connected to the input/output bus include:-

1. Readers, Punches, printers, plotters and display units, as listed in section 3.6.2. For every group of eight such units, an input/output controller is required.
2. Multiplexors, each providing up to 32K inputs and/or outputs of 8 bits for process control.

2.4 MULTI-PROGRAMMING

Any system which includes more than one block of external core store is capable of operating in a multi-programming mode. That is, a number of separate programs can operate concurrently, each program having a level of priority which is allocated by the operator. The number of programs which can run concurrently is equal to the number of external blocks of store provided in the system.

The program which has control of the processor at any instant is that program which is of highest priority of those programs which are ready to take control. A program is deemed to be ready to take control of the processor if it has available all the data and peripheral devices which it needs at that moment to perform its required function. When a program becomes unready due to unavailability of data on peripheral devices, then the next highest priority program of those which are ready assumes control.

Priority control of multi-programs is a function of Executive, and the individual users programs do not themselves differ in any way from those which run on a single program machine. Executive ensures that programs cannot interfere with each other, and that no user can 'steal' data from another users program unless this has been specifically authorised.

2.5 MULTI-ACCESS

A facility which is desirable, if not essential in a multi-programming system, is multi-access. This means that two or more operators can concurrently but independently access the processor from their own particular input/output devices, either each controlling his own programs, or all controlling the same programs. K-202 provides for up to 64 separate access peripherals.

2.6 MULTI-PROCESSORS

It is possible to connect up to four, or in some cases more, processors to the same bus, so that they share the same operating memories and bulk store, and may or may not share the same input/output peripherals. The advantages of this multi-processor system are:-

1. All processors have access to the same central data store, as is required in a Total Management system.

2. Systems software library is available to all processors, and is not separately stored for each.

3. Each processor has its own Executive program, which will be smaller and very much faster than that required for a single, large processor of the same computing power.

4. An overloaded system may be expanded by additional processors, without any change in techniques or systems as an organisation expands.

3. MODULES OF THE SYSTEM

This section describes the hardware modules which make up a K-202 system.

The processor as described in 3.1 is a complete computer in its own right, in that it includes basic power supplies, control panel, the basic minimum amount of core store, and an input/output controller. Add to this a peripheral device such as a teleprinter, and it becomes the minimum useable system, as described in section 2.2.

The remainder of section 3 goes on to describe the other modules which may be connected in any combination to this basic computer in order to build it up into a large and comprehensive system.

3.1 PROCESSOR

The processor can be considered in five parts:-

1. Register System with arithmetic unit
2. Control Logic
3. Interrupt priority logic
4. The internal store
5. The internal I/O Controller

3.1.1 Register System

All registers are connected to the internal bus, which is in turn connected to the external bus. This system provides the universal means of data transfer both inside and outside the processor.

Ten registers are directly available to the programmer. These are:-

RO - Which holds the set of conditions upon which conditional orders depend.

(Rl to
(
(R7 - Universal registers which serve as accumulators, modifiers, indexes, or pointers as required.

IC - The instruction counter.

BAR - The block address register. This holds the address of the block of store in current use.

A further six registers are used in the logic, but are not directly available to the programmer. They are:-

AA & AC - Which hold the two operands at the input to the adder.

AT - Output register for the adder.

IR - The instruction register.

AR - The address register.

BIR - Holds the peripheral status word.

3.1.2 Control Logic

The control logic decodes the instructions and uses the information obtained to generate register gating and other signals to control the adder, store and peripheral logic.

Control of each instruction is achieved by generating in the logic a series of micro-instructions. The logic is switched consecutively through a series of 'states'. A state is said to exist/...

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exist when one of the 24 state bistables is set, only one of which can be set at any time.

The purpose of each state bistable is to generate a number of gating, control and conditioning signals, which are levels, not pulses. Of the signals which it can generate, some are inhibited at any time dependent upon conditions set up earlier.

The first state to be set for a given instruction depends upon a decode of the bits of the instruction, together with conditions prevailing at that time in registers and on control and peripheral lines.

Choice of the next state depends upon similar parameters plus the presence of all the signals which should have been generated by the first state.

Any state may be used more than once in the chain, its effect differing each time according to the conditions set up earlier. An instruction chain may contain any number of states.

There is no central timer. The amount of time that a state remains set is simply that amount of time that it requires to generate its control signals. A logical sum of these forms the signal which steps to the next state.

Thus the system is fail safe: it cannot proceed to the next state until the first one has been completed satisfactorily. If signals are slow to come up, the system waits for them; if they fail to come up, the system stops. When this happens, a monostable terminates the faulty state after a few microseconds delay, and brings up the next state, but at the same time it generates an error signal to show where the fault occurred. The system can be stopped at any intermediate stage of the instruction chain by inhibiting any signal, leaving all signals available as steady, D.C. levels for inspection.

The resultant system is extremely fast in operation, completely asynchronous, and faults are self-diagnostic.

3.1.3 Interrupt Priority Logic

Thirty two levels of priority are provided in the interrupt system of the basic machine. This can be extended to sixty four levels, and each level can cater for up to sixteen sub-levels of priority.

The basic 32 levels are normally allocated in blocks of 8. The eight highest levels of priority are given to the system error interrupts. The next eight to the bulk store controllers; the third block of eight are allocated to the input/output controllers, and the last block are available for any other devices which may be connected to the bus. Each input/output controller and store controller has eight sub levels of interrupt priority to cater for the eight devices it controls.

The chances of all interrupts occurring simultaneously are so remote as to be virtually non-existent, but if they did, then the one of lowest priority would be kept waiting only micro-seconds before being serviced.

3.1.4 Internal Store

At least one block of core store is essential in even the smallest system. This is called block 0 and is located inside the cabinet of the processor. It may vary in size from 4K to 16K words of 16 bits, and its cycle time may be 0.7 uS or 1.2 uS depending upon the requirements of the system. Apart from its location within the processor, and its limited size, it is in all other respects similar to the external stores described in section 3.4.

3.1.5 Internal I/O Controller

Of the various input/output controllers which may be fitted to the K-202, at least one is essential in even the smallest system. This is called I/O Controller no. 0 and is fitted inside the cabinet of the processor. Unlike the other controllers, the internal controller handles only four devices. However, it may be extended to eight devices by installing the additional logic external to the cabinet. Logically, it is similar to the external I/O controllers. Each device that it handles may be for input or output or combined input and output

3.2 FAST ARITHMETIC UNIT

The fast arithmetic unit is an option which may be provided with the processor. If fitted, it goes inside the processor, occupying seven logic board positions.

The function of this unit is to carry out multiplication, division, and floating point operations by hardware. It is about 36 times faster than the extracode instructions which would otherwise carry out these operations.

The inclusion of a fast arithmetic unit in a processor makes no difference to the programming. The program simply calls for the operation it requires, and Executive will utilise the fast arithmetic unit if fitted, but otherwise will automatically call up Extracode.

3.3 THE DUAL BUS

Two independent bus systems are provided. One caters for transfer of whole words, and is used primarily for communications between the processor, core store modules, and bulk storage peripherals. The other caters for transfer of eight-bit characters and is used by the processor to communicate with input/output devices. Both are connected to the internal bus, which in turn is connected to all the registers. The overall system of buses provides the universal means of communication both inside and outside the processor.

3.3.1 Why Not a Single Bus?

For simplicity and economy it is convenient to use a single bus on small computers. However, where a system has the expansion capabilities of the K-202, a single bus suffers from a number of inherent disadvantages.

(a) Where store cycle time is so short as to be of the same order as the time taken to transfer a word via the bus, then the bus becomes fully loaded with a single transfer, and no other data transfers can take place simultaneously, without slowing down the original transfer.

(b) The user cannot be given freedom to attach any peripheral of his choice to a single bus, because unbuffered peripherals would stop the processor for relatively long periods by occupying the bus whilst preparing to accept or transmit their data. Providing a buffer increases the cost of peripheral interfaces.

(c) Most input/output devices require only eight bit character transfers. The apparent economy of a single bus system is offset by the cost of cables and interfaces which provide for the transfer of 16 bits, half of which are not required.

For these reasons it was decided to utilise the more complex dual bus system. The store bus handles word transfers between the processor and blocks of store, including bulk storage units such as drums, discs and magnetic tape. The input/output bus deals exclusively with input and output character transfers, and should it be held up by a peripheral, the processor and store are not affected.

3.3.2 The Store Bus

The store bus consists of fifty pairs of balanced lines which are common to the processor, all core stores and bulk store controllers. Of these lines, 16 carry a word of data, 16 carry the address, 8 carry the block number and the remaining 10 are control and interrupt lines.

All transfers via the store bus are autonomous. That is, they are initiated by the processor, but then take place automatically whilst the processor carries on with other work. When the transfer of a whole block of words is complete, the processor will receive an interrupt to signal that the data is now available at its destination.

Any number of data transfers can take place simultaneously, the various store controllers alternating in their use of the bus; as each store goes through its read/write cycle, it releases the bus for others to use.

Time taken for each data transfer is approximately one microsecond per word, but this can vary as the system is asynchronous. Stores with a slow cycle time will of course transfer data only as fast as the store itself can work.

3.3.3. Input/Output Bus

The input/output bus consists of 29 pairs of balanced lines which are common to the processor and all input/output controllers. Of these lines, 8 carry a character of data, 6 carry an address which consists of two octal numbers identifying controller and device, respectively, and the remaining 15 are control and interrupt lines.

All transfers via the input/output bus operate on a time sharing basis. That is, the users programs can call for transfer of different blocks of characters to or from any number of peripheral devices, and they will all take place simultaneously, without stopping the users programs from running; the various devices alternating in their use of the bus. The Executive program keeps a record of the progress of these transfers, and informs the various users programs when each block of data has been input or output as required.

Time taken for each character transfer is approximately one microsecond but of course the time interval between transfer of two consecutive characters will depend upon the speed of the peripheral device itself.

3.4. CORE STORES

From one to sixty-four blocks of 16 bit ferrite core store may be fitted to a K-202 system, numbered 0 to 63 inclusive, this number being the address of the block for programming purposes.

Block 0 is essential in even the minimum system. It is located in the processor cabinet and is described in the processor section.

The remaining 63 blocks may each be from 16K to 64K words, with cycle times of 0.7 uS or 1.2 uS, access time being about half this figure in each case. Operation is on the 3 wire principle.

Each block is mounted, together with its power supplies in a frame which fits into a cabinet similar to that which houses the processor; or it may be mounted in a standard 19" rack. Three connectors are provided on each store module: a mains power connector, and bus input and output connectors. Where a block of core store is the last module on the bus, its bus output will be connected to a matched line terminator.

3.5 STORE CONTROLLERS

The function of a store controller is to control up to eight magnetic disc, drum or tape units. These may be identical units or a mixture of the different kinds. The controller is housed in a frame similar to the one which holds the processor. Eleven connectors are provided; these are bus input and output, mains power input, and eight connectors for the peripheral devices.

When a program calls for transfer of data between a bulk storage peripheral and a block of core store, the processor sends the request to the relevent store controller via the store bus. The controller then transfers the block of data via the bus, whilst the processor carries on with its other work. When the transfer is complete, the controller sends an interrupt signal which informs the processor that the data is now available at its destination. Each controller can handle transfers to or from all of its eight devices simultaneously; and all controllers can operate at the same time. An individual level of interrupt is provided for each controller, and within the controller is logic which allocates sub-levels of interrupt priority to each of the eight devices.

3.6 INPUT/OUTPUT CONTROLLERS

The function of an input/output controller is to control up to eight input/output peripherals. These may be any combination of three kinds of device: input devices, such as paper tape or card readers; output devices such as punches or printers; or combined input/output devices, such as typewriters, teleprinters and digital display units.

The controller is housed in a frame similar to the one which holds the processor. Eleven connectors are provided; these are bus input and output, mains power input, and eight connectors for the peripheral devices.

The processor may transfer a character of data to or from any device, via the controller, and when the device is ready to send or receive the next character it will interrupt the processor to request the next transfer. In this way, all eight devices can transfer blocks of data simultaneously. An individual level of interrupt is provided for each controller, and within the controller is logic which allocates sub-levels of interrupt priority to each of the eight devices.

4. PRINCIPLES OF OPERATION

This section describes how instructions and data are stored in the K-202, and how they are used in a single program. It then goes on to explain how several programs can run concurrently, and to describe the interrupt and program priorities which facilitate this. An introduction is given to the Executive program, who's function is to control the users programs and keep a record of their progress.

4.1 COMPUTER WORD

A K-202 computer word consists of 16 binary bits numbered 0 to 15 from left to right.

In double length numbers, two computer words are effectively placed end to end to produce a 32 bit word in which the bits are numbered 0 to 31 from left to right.

These numbers are used only for identification of bits, and bear no relation to the binary value of the individual bits.

4.2 FORMAT OF INSTRUCTIONS

WORD 1	OP	W	D	A	B	C
WORD 2	WC					
WORD 3	M					
WORD 4	E					

Variable length instructions occupy from one to four words. Word 1 is essential in all instructions, words 2 to 4 are optional. If used, they appear in the order shown; if omitted, then the following words move up, i.e. M could appear as word 2 in a two word instruction, and E could appear as words 2 or 3 in a two or three word instruction.

OP (5 bits) Specifies which basic operation is to be carried out.

W (1 bit) If W = 1 then the instruction is conditional.

D (1 bit) If D = 1 then the second operand is indirect.

A (3 bits) Specifies which general register holds the first operand.

B (3 bits) Specifies which general register holds an index for the second operand. If B = 0 then no index is required.

C (3 bits) Specifies which register holds the second operand. If C = 0 then the second operand will be found in M.

WC (16 bits) Is the mask which is used for checking the conditions register RO if W = 1

M (16 bits) Holds the second operand if C = 0

E (16 bits, of which bits 0 to 7 are not used)
Holds the name of an extracode.

N.B. In practice, most orders require only one word, and very

4.2.1 Conditional Instructions

If W = 1 in the instruction, then the mask held in WC will be checked against the contents of the conditions register RO, and the instructions will be carried out only if RO contains ones in the bit positions where the mask contains ones; otherwise, the instruction will be skipped.

If W = O then the instruction is not conditional, and WC must be omitted from the instruction.

Layout of bits in the Conditions register, RO:

Q	L	E	G	V	C	Y	I	X							

9 bits set by hardware

8 bits available to programmer

N.B. X can be set by hardware or the programmer.

The conditions register RO has nine bits set by hardware to record the information shown below. X and the other seven bits may be set by the programmer for use as flags or indicators. RO is used in conditional instructions to compare with a mask set by the programmer, and the instruction is carried out only if the comparison is valid.

Q - If Q = O then block zero of store in use and BAR does not modify addresses.

L -)
) In the last comparison, operand II was less than/
E -)
) equal to/greater than operand I.
G -)

C - Carry

V - Overflow

Y - Holds the bit which overflows at either end of the register during shift instructions.

I - Interrupts allowed if I = O.

4.2.2 Indirect Operands

If D = 1 then the second operand is indirect; that is to say, the number found in M, or in the register specified in C, is not the operand itself. Instead, it is the address of a store location which holds the second operand.

4.3 FORMAT OF DATA

Numbers are represented in fractional form, negative numbers being held as their two's complement. The degree of accuracy with which a number can be represented depends upon the quantity of bits used to describe it.

4.3.1 Single Length Numbers

Single length numbers utilise 16 bits. Of these, bit 0 is the sign digit and the remaining 15 bits represent the number. Positive numbers can be represented with an accuracy of one part in 65,535 negative numbers to a slightly higher degree of accuracy.

4.3.2 Double Length Numbers

Double length numbers utilise 32 bits. Of these, bit 0 is the sign digit and the remaining 31 bits represent the number. Positive numbers can be represented with an accuracy of one part in 4,294,967,295 negative numbers to a slightly higher degree of accuracy.

4.3.3 Floating Point Numbers

Floating point numbers are held in the form $N = A \times 2^b$, where the mantissa, a, is held as a double length number; and the exponent, b, is held as a single length number. The largest number which can be accurately represented in this form is so great that this whole book is not large enough to hold it in print!

4.3.4 Format of Text

Text consisting of upper and lower case letters, numbers, and other symbols is stored in ISO 7 code, two characters per word.