PATENT SPECIFICATION (11) 1 480 209

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(21) Application No. 16685/73 (22) Filed 6 April 1973

(23) Complete Specification filed 3 July 1974

((44) Complete Specification published 20 July 1977

(51) INT. CL.[2] G06F 9/00

(52) Index at acceptance
G4A 13E 16D 6M1 PX

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(19)

(54) IMPROVEMENTS IN OR RELATING TO DIGTAL COMPUTERS

(71) We, DATA-LOOP LIMITED, a British company of 1 Golden Court, Richmond, Surrey TW9 1EU, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to improvement in digital computers and is especially concerned with the provision of an improved computer including a facility which gives substantial advantages in flexibility of programming.

The inclusion of this invention in a computer simplifies and makes more flexible its programming procedures, and enables programmes to be written which utilise less store space and less computation time than they would otherwise require.

The invention provides a facility whereby the programmer can make any or all of the instructions in a programme conditional. This is, each instruction can be specified such that it will be executed only if certain predetermined conditions exist in the computer, and will be ignored if they do not exist. Furthermore, the condition or set of conditions which must exist to permit execution of a given instruction can be specified by the programmer individually and differently for each and every instruction.

According to the present invention there is provided a digital computer including data processing means arranged to perform operations commanded by an instruction word applied thereto on data therein, a store containing a plurality of said instruction words, programme-controlled means for applying said instruction words selectively to command said data processing means, a condition registor containing a condition word comprising a plurality of bits representative of conditions which are or have been present within the computer and of its programme, wherein said data-processing means is arranged to execute forthwith the command contained in an instruction word applied thereto unless a 1 bit is present in a specified position in a chosen register of said computer, in which case said data processing means is arranged to execute said command only if the word in said condition register contains 1 bits in all positions in which 1 bits are present in a subsidiary instruction word, of the same length as said condition word, which is associated in said instruction store with said main instruction word.

Preferred features of and advantages obtained by the use of the invention will become apparent from the following description of an embodiment thereof, taken in conjunction with the accompanying drawings of which:

Figure 1 illustrates the format of an instruction which may be contained in a computer programme;

Figure 2 illustrates the condition register of a computer;

Figure 3 is a flow diagram illustrating the response of the computer to the instruction illustrated by Figure 1; and

Figure 4 is a block diagram illustrating the computer functions necessary for carrying out the invention.

A computer into which this invention has been embodied includes the following characteristics.

Referring to Figure 1, each instruction of a programme, when held in the store of the computer, occupies a main instruction word 1 of 16 bits, and may also occupy a plurality of subsidiary instruction words 2 each of 16 bits. For the purpose of describing this invention, we are concerned only with a single bit here called W, in the main instruction word; and with the whole of one subsidiary instruction word here called WC.

These are denoted by shading in Figure 1.

The computer contains a 16 bit condition register 3, Figure 2, in the course of normal operation of the computer a number of the bits in this register are automatically set by the computer logic circuits to record the occurrence of certain events; for example, one particular bit 4 may be set if the arithmetic unit overflows; another bit 5 is set if the result of any calculation is zero and so on. Other bits in the condition register, such for example as 6, 7, 8, may be set by the programme, each bit recording the occurrence of any event the programmer cares to assign to it. Thus, any combination of sixteen different conditions which have occurred as a result of the functioning of the computer and its programme can be represented in the condition register.

When writing a programme, the programmer indicates that instruction is to be conditional by setting its W bit equal to 1, and specifying the contents of its WC word. In conditional instructions this word must be specified such that it contains a replica of what the condition register is required to contain in order to justify execution of that particular instruction.

Referring to Figure 3, the computer holds the programme of instructions in its store, and extracts and executes them sequentially. After it has extracted each instruction from store (block 11) and prior to executing it the logic circuits of the computer examine the W bit (block 12) to see if it is set to 1. If it is, then the associated WC word is extracted from store and applied to an input of a function unit (block 13). The contents of the condition register are applied to another input of the function unit (block 14), which is then used (block 15) to compare the WC word with the contents of the condition register; the instruction is then executed (block 16) if the condition register contains 1 bits in positions corresponding to those in which the WC word contains 1 bit, otherwise it is ignored (block 17).

The next step in the programme is then performed (block 18) a simplified block diagram of the apparatus used to carry out the testing of W and validation of the WC word as shown in Figure 4.

A control logic unit 20 generates at C a number of control signals which are routed variously to the logic gates and other elements of the system, which they enter at points marked C. The relative timing and destinations of these signals causes the necessary flow of information, as follows.

A main instruction word is read from a core store 22 into store register 23 and gated into instruction register 25 via data bus 24 by opening gates 22 and 21, at this point the W bit is tested by a test circuit 26, which if W=0 generates a signal at point 0 which allows the 'execute' sequence to commence. If W=1 then test circuit 26 generates a signal at I which causes the control logic 19 to enter a validation sequence.

In the validation sequence, the WC word for this instruction is read from core store 22 into the store register 23 and gated via the data bus into input A of a function unit 70 by opening gates 21 and 27.

The contents of the condition register 80 are then gated via the data bus 24 to input B of the function unit by opening gates 28 and 29.

In the function unit the two words at inputs A and B are compared to produce a VALID signal in an output line 30 if the comparison is valid, or an INVALID signal on an output line 31 if the comparison is invalid.

The VALID signal if produced is routed to the control logic unit through gates 32 and 33 and causes the computer to enter the 'Execute' sequence.

The INVALID signal is routed to the control logic unit through a gate 34 and causes the computer to extract the next instruction; thus completely omitting the execution sequence for the conditional instruction for which the condition word was invalid.

In a modification of the arrangement described above the validation sequence may be arranged to be initiated by the presence of a "1" bit placed in a specified position in some other register of the computer in the course of operation in response to a previous instruction.

In another modification the subsidiary instruction word is not necessarily a constant word permanently associated with a given instruction word, but may be set up, in the course of operation in response to one or more previous instructions, in a position in the instruction store from which it is always withdrawn in succession to a given instruction word, when said 1 bit is present in said specified position.

Advantages which are gained by the use of the present invention are:

Each and every instruction can be made conditional or not as required; in most computers only certain instructions are conditional, and those instructions cannot be made unconditional.

An unlimited variety of conditions or combinations or conditions can be made the deciding factor as to whether any given instruction should be executed or skipped.

In most computers only one condition can decide whether a given instruction is to be executed or skipped.

WHAT WE CLAIM IS:

1. A digital computer including data processing means arranged to perform

operations commanded by an instruction word applied thereto on data therein, a store containing a plurality of said instruction words, programme-controlled means for applying said instruction words selectively to command said data processing means, a condition register containing a condition word comprising a plurality of bits representative of conditions which are or have been present within the computer and of its programme, wherein said data-processing means is arranged to execute forthwith the command contained in an instruction word applied thereto unless a 1 bit is present in a specified position in a chosen register of said computer, in which case said data processing means is arranged to execute said command only if the word in said condition register contains 1 bits in all positions in which 1 bits are present in a subsidiary instruction word, of the same length as said condition word, which is associated in said instruction store with said main instruction word.

2. A digital computer in accordance with claim 1, wherein said specified position of said 1 bit is a position in said main instruction word.

3. A digital computer in accordance with claim 1 wherein said data processing means includes means arranged to transfer from said instruction store successive ones of said main instruction words contained therein, means arranged as each main instruction word is transferred to test said specified position of said chosen register for the presence of a "1" bit, means responsive to the presence of a "1" bit in said specified position to apply to an input of a function unit in said data-processing means a subsidiary instruction word associated with the transferred main instruction word, to apply the condition word contained in said condition register to another input of said function unit, and to cause said function unit to compare each digit of said subsidiary instruction word with the corresponding digit of said word in said condition register, to cause said instruction to be executed if 1 bits are present in all positions of said condition word at which 1 bits are present in said subsidiary instruction word and to cause said main instruction word to be replaced by the succeeding main instruction word in said store otherwise.

4. A digital computer in accordance with claim 2 wherein said instruction store is associated with a store register into which instruction words contained in the instruction store may be transferred in succession, said computer further including an instruction register, a test circuit, a control logic, a data bus by way of which an instruction word contained in said store register is, under the control of signals from the control logic, fed into the instruction register and applied to the test circuit, the test circuit being arranged to test the word for the presence of a 1 bit in said specified position and if said bit is present to generate a signal causing the control logic to enter a validation sequence in which the subsidiary instruction word associated with the main instruction word in the instruction register is transferred by way of the data bus to a first input of a function unit, the condition word contained in the condition register is transferred by way of the data bus to another input of said function unit wherein the two applied words are compared to generate a valid signal if 1 bits are present in all positions of said condition word at which 1 bits are present in said subsidiary instruction word and an invalid signal if otherwise, the valid signal causing the instruction represented by the word in the instruction register to be executed and the invalid signal causing the word in the instruction register to be replaced by another main instruction word contained in the instruction store.

5. A digital computer in accordance with claim 1, 2 or 3 arranged so that each said subsidiary instruction word is arranged to be set up, in the course of operation of the computer in response to one or more previous instructions, in a position in said store from which it is always withdrawn in association with its associated main instruction word, when said "1" bit is present in said specified position.

6. A digital computer constructed and operating substantially as described with reference to the accompanying drawing.

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Printed for Her Majesty's Stationery Office by The Tweeddale Press Ltd., Berwick-upon-Tweed, 1977.
Published at the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1480209 COMPLETE SPECIFICATION
2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 1

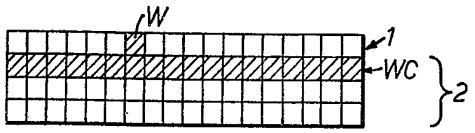

FIG.1.

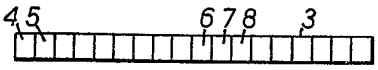

FIG.2.

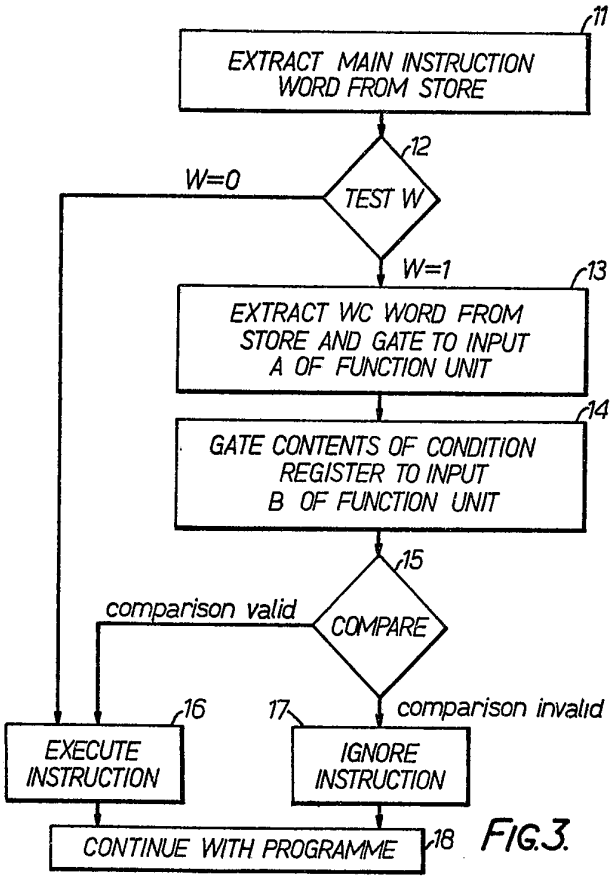

FIG.3.

1480209 COMPLETE SPECIFICATION
2 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheet 2

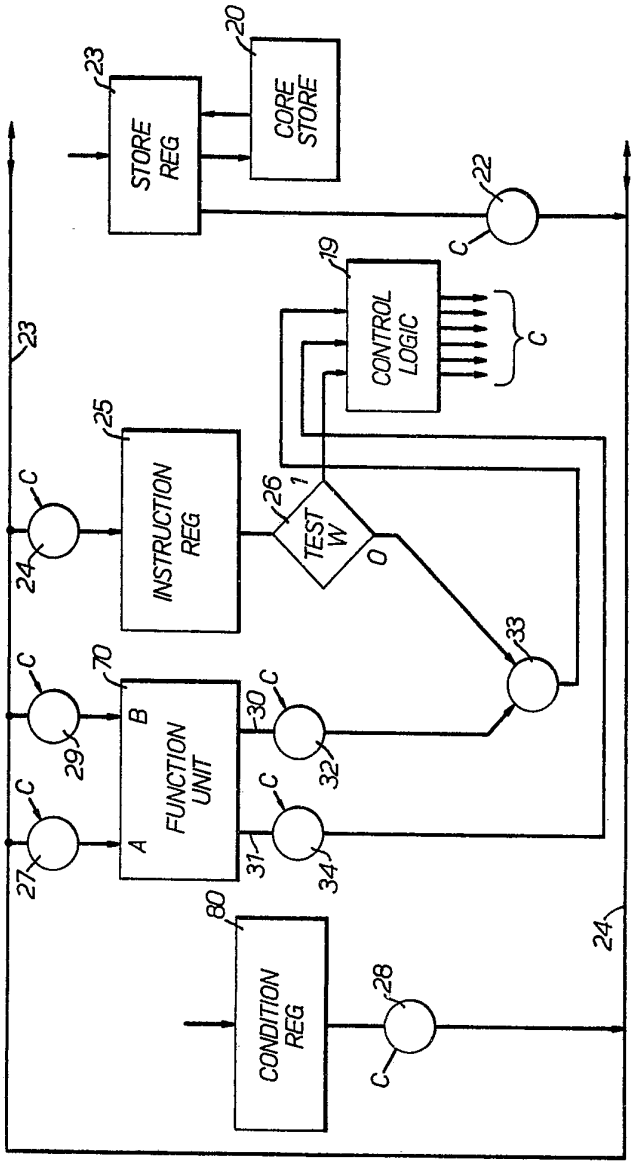

FIG.4.