PATENT SPECIFICATION (11) 1 480 208

1 480 208

(21) Application No. 16684/73 (22) Filed 6 April 1973
(23) Complete Specification filed 3 July 1974
(44) Complete Specification published 20 July 1977
(51) INT. CL.[2] G06F 3/00
(52) Index at acceptance
G4A FK PR

(72) Inventor JACEK KARPINSKI

(19)

(54) IMPROVEMENTS IN OR RELATING TO DIGITAL COMPUTERS

(71) We, DATA-LOOP LIMITED, a British company of 1 Golden Court, Richmond Surrey TW9 1EU, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to an improved arrangement for data transfer between computer units using a common data bus to which a data processor unit and a plurality of external data storage and peripheral units are connected. Arrangements are known in which data may be automatically transferred from one such unit to another while the computer is performing other functions. It is possible that data is available to be transferred between several pairs of units at the same time and it is therefore necessary to provide a means which will permit all such transfers to take place with a minimum of mutual interference and preferably in the shortest possible time.

A known arrangement for permitting such transfers uses a priority logic system frequently located in the data processor. Each external unit from which it may be required to transfer data to another unit has an individual request line connected to the priority logic system and when the need arises for data to be transferred from any unit a request is sent to the priority logic along the respective line. The priority logic then allocates control of the bus to that unit. Whenever two or more units request the bus simultaneously the logic allocates the bus to each in turn in accordance with a built-in set of priorities.

There are two prime disadvantages of this arrangement. Firstly, any expansion of the computer by the addition of additional units involves making changes to the priority logic system in the processor and the addition of extra lines to the bus, with resultant expense and the inconvenience of computer down-time while the change is being made. Secondly, the built-in fixed priorities being unchangeable during operation it may be found that for certain operations some of the units of low priority will be unable to obtain access to the bus in a reasonably short time owing to pre-empting by units of higher priority.

The present invention seeks to provide a means of bus allocation which does not require the inclusion of purpose-built logic in the processor, so that expansion of a computer may be effected without changes in the processor itself or the bus. The arrangement according to the invention also avoids the necessity to allocate priorities to the different units, all of which may have an equal chance of obtaining control of the bus when it is demanded by different units simultaneously.

According to the present invention there is provided a digital computer including a data processing unit and a plurality of ancilliary units all inter-connected by a common data bus for transfer of information between said units, each of said units being arranged in response to the appearance of an individual address code on a set of address lines included in said bus to assume a data-receptive condition, wherein said data bus includes a busy line common to all said units and each said unit is arranged, when it contains data required to be transferred to another said unit, to test whether a set signal is on said busy line, and if so cyclically to repeat the test until the busy line is found not to have a set signal thereon, and thereupon and if the busy line did not have a busy signal thereon to apply a set signal to the busy line and to apply its own individual address code, the number of digits in which corresponds inversely to the unit priority to

said address lines, each address of lower priority differing from an address of higher priority only in respect of digits additional to those of the address of higher priority, to test if the address on the address lines corresponding to said number of digits is correct, if the address is not correct to revert to testing the busy line, and if the address is correct to remove said address code from the address lines and to apply thereto the address code of the unit to which data is to be transferred and thereafter transferring the data while maintaining the set signal on the busy line until data transfer is complete.

The invention will be better understood from the following description taken in conjunction with the accompanying drawings, in which:—

Figure 1 is a schematic diagram illustrating a known bus accessing arrangement used in digital computers;

Figure 2 is a schematic diagram illustrating a bus accessing arrangement in accordance with the invention;

Figure 3 is a diagram illustrating the functioning of a bus accessing arrangement in accordance with the invention; and

Figure 4 is a diagram used to described the operation of a digital computer in accordance with the invention.

In the known arrangement shown in Figure 1 a computer data processor 11 and a plurality of ancilliary units 12, 13, 14 are all connected to a common data transfer bus 15, over which data may be transferred from any one unit to any other, as may be required. When it is required to transfer data from one of the units 12, 13, 14, this unit applies a signal by way of a respective request line 12*a*, 13*a*, 14*a* to a priority logic system 16, conveniently located in data processor 11 which signals to the requesting unit the proper time for that unit to use the bus.

Figure 2 illustrates an arrangement in accordance with the invention in which a data processor 21 and additional units 22, 23, 24 are again connected by way of a common data transfer bus 25. In this case, however, data bus 25 contains in addition to numerous data transfer and control lines (not shown) a common busy line 27 which also is connected with the processor 21 and with each of the units 22, 23, 24.

When a unit has data to be transferred to any other unit, the procedure shown in Figure 3 is followed. The first operation, represented by block 31 is to test if the busy line has a set signal already applied to it by another unit. If this is the case the unit continues to test the busy line until the set signal is removed. When the busy line is free the unit itself applies a set signal to the line and, as indicated by block 32, applies to a set of unit address lines 28 forming a part of the bus 25, signals uniquely denotive of its own address.

Figure 4 illustrates addresses denotive of access priority which are advantageously used as denotive of three units A, B and C. Each address comprises in this embodiment a unique code consisting of 0 bits except for a single 1 bit, of which the order is chosen in accordance with the priority of access which is to be given to the unit; the nearer the commencement of the word, the higher the priority. Thus the address of unit A consists of a single 1 bit following five 0 bits so that five other units may be given higher access priority than unit A, unit B has a priority lower by two digits than that of unit A and unit C has a priority lower by three digits than that of unit B.

A test is then applied, as shown by block 33, to determine that the address actually appearing on the unit address lines 28 is in fact the correct address of the unit. Each unit is arranged to test only that part of the address word extending to and including its own address digit, as indicated by brackets A′, B′, C′ in Figure 4.

It will be understood that each unit will determine the address on the address line as being correct provided that any unit of which the address is simultaneously applied to the address line is of lower priority, and will determine the address as incorrect if the address of a unit of higher priority is simultaneously present on the address line.

If the tested address is correct, then as indicated by block 34 the address applied to the lines 28 is removed while the set signal on busy line 27 is maintained. Data is then transferred in a normal manner as required, using the unit address lines as required, as shown by block 35, and when data transfer is complete the set signal is removed from busy line 27, leaving the bus free for access by other units.

If the test applied in block 33 shows that the address appearing on the unit address lines is not the correct address of the unit seeking access, this must be because another unit of higher priority has simultaneously sought access to the bus, so that the addresses of both units are on the lines 28. In this case, as indicated by block 37 the unit removes its own address and the busy signal from the unit address lines 28 and then reverts to the condition of testing the busy line, the cycle being repeated until the unit obtains access to the bus.

WHAT WE CLAIM IS:

1. A digital computer including a data processing unit and a plurality of ancilliary units all interconnected by a common data

bus for transfer of information between said units, each of said units being arranged in response to the appearance of an individual address code on a set of address lines included in said bus to assume a data-receptive condition, wherein said data bus includes a busy line common to all said units and each said unit is arranged, when it contains data required to be transferred to another said unit, to test whether a set signal is on said busy line, and if so cyclically to repeat the test until the busy line is found not to have a set signal thereon, and thereupon and if the busy line did not have a busy signal thereon to apply a set signal to the busy line and to apply its own individual address code, the number of digits in which corresponds inversely to the unit priority, to said address lines, each address of lower priority differing from an address of higher priority only in respect of digits additional to those of the address of higher priority, to test if the address on the address lines corresponding to said number of digits is correct, if the address is not correct to revert to testing the busy line, and if the address is correct to remove said address code from the address lines and to apply thereto the address code of the unit to which data is to be transferred and thereafter to transfer the data while maintaining the set signal on the busy line until data transfer is complete.

2. A digital computer in accordance with claim 1 wherein the address code of each of said units comprises a sequence of 0 digits containing a single 1 digit, the position in the code of the single 1 digit corresponding to the access priority to be given to that unit, and each unit is arranged to test for correctness only that portion of the address word extending to the 1 digit constituting its own address.

3. A digital computer including a data processing unit and a plurality of ancilliary units all interconnected by a common data bus for transfer of information between said units, constructed and arranged to operate substantially as herein described with reference to Figures 2, 3 and 4 of the accompanying drawings.

A. A. THORNTON & CO.,
Chartered Patent Agents,
Northumberland House,
303-306 High Holborn,
London. W.C.1.

Printed for Her Majesty's Stationery Office by The Tweeddale Press Ltd., Berwick-upon-Tweed, 1977.
Published at the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

1480208 COMPLETE SPECIFICATION
2 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheet 1

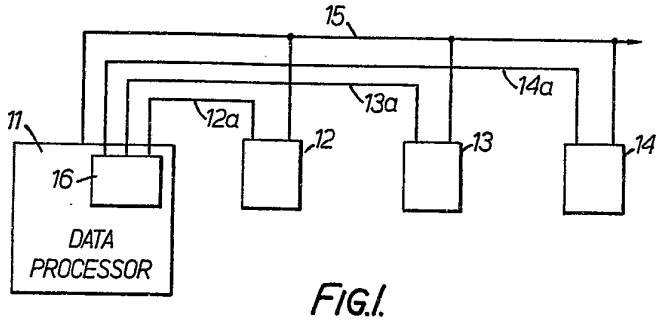

FIG.1.

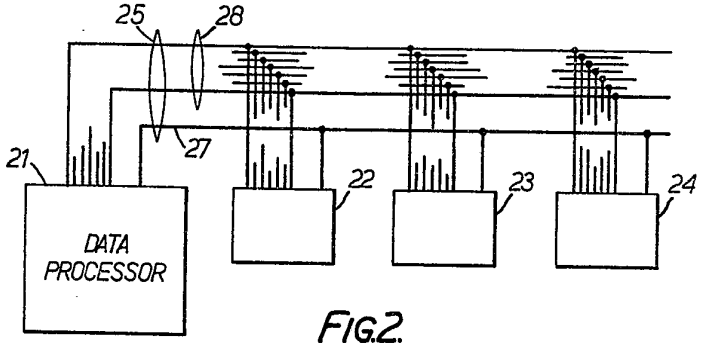

FIG.2.

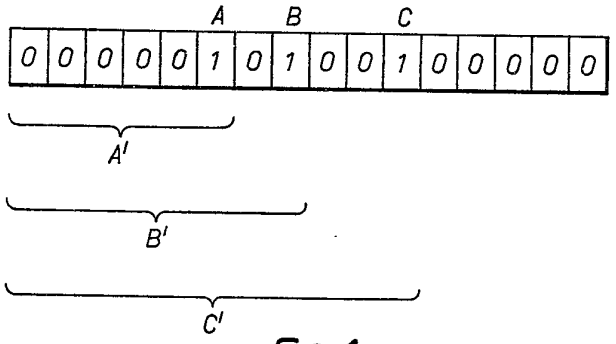

FIG.4.

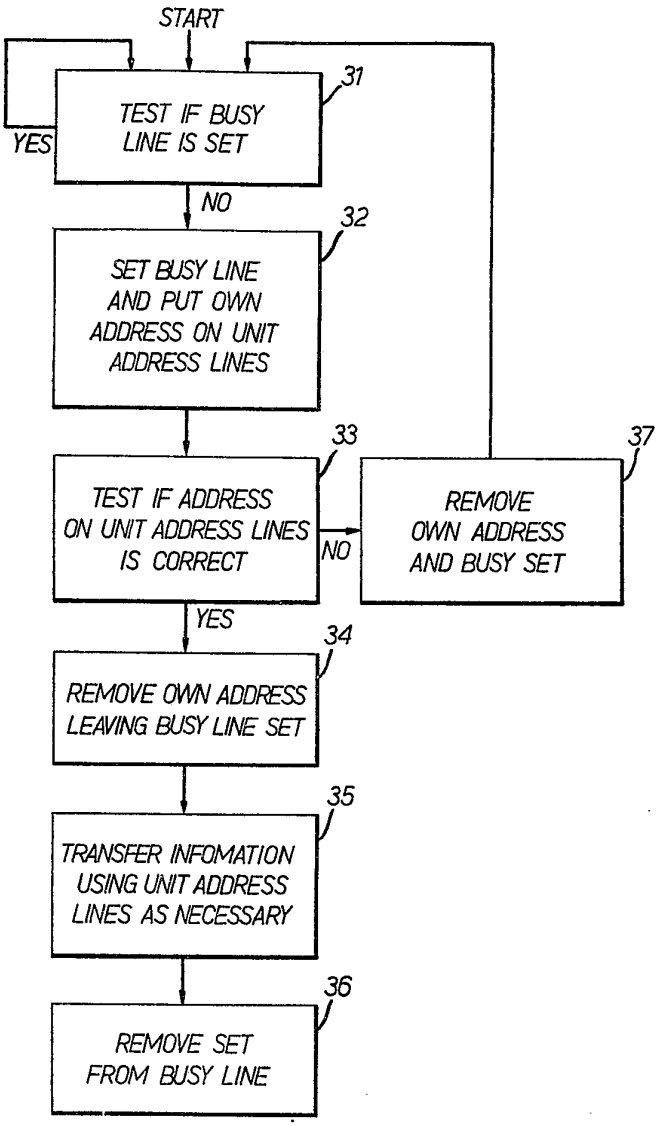
START
TEST IF BUSY LINE IS SET
31
YES
NO
SET BUSY LINE AND PUT OWN ADDRESS ON UNIT ADDRESS LINES
32
TEST IF ADDRESS ON UNIT ADDRESS LINES IS CORRECT
33
NO
REMOVE OWN ADDRESS AND BUSY SET
37
YES
REMOVE OWN ADDRESS LEAVING BUSY LINE SET
34
TRANSFER INFOMATION USING UNIT ADDRESS LINES AS NECESSARY
35
REMOVE SET FROM BUSY LINE
36

FIG.3.